SWITCH MODE POWER SUPPLY AND DRIVING METHOD FOR EFFICIENT RF AMPLIFICATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to switch mode power supplies and driving methods, particularly for efficient RF amplification, as well as amplifier structures using the same.

2. State of the Art

As is well-known, the efficiency of power amplifiers such as those used in wireless telecommunications can be increased substantially using a variable power supply instead of a fixed power supply. In this application, as well as a wide variety of other applications, a switch mode power supply may be used to efficiently perform DC-to-DC conversion from a fixed DC power supply input to a variable supply output.

One example of a known switch mode power supply (in particular a buck converter) and associated driver circuit is shown in Figure 1. A transistor switch Q5 (in this instance a N-FET device) is alternately switched ON and OFF in accordance with some duty cycle during an ON portion of which an operational voltage V_{DD} is coupled to an output filter. The output filter may take the form of a series LC circuit, where the output voltage is taken at a circuit node N in-between an inductor L1 and a capacitor C2. In addition, a Schottky diode D1 is provided to clamp the negative voltage spike induced in the inductor when the switch is turned OFF, forcing the output voltage positive and protecting the transistor Q5.

A driving circuit for the buck converter includes a high-side driver/level shifter 110 and a low-side driver 120.

The low-side driver 120 includes a transistor switch Q2 coupled between a gate electrode of the transistor Q5 and a reference potential, e.g., ground. During the OFF portion of the duty cycle, the transistor Q2 is turned on, grounding the gate of the transistor Q5, causing it to turn off. A gate electrode of the transistor Q2 may be driven directly by a control circuit or, as in the illustrated embodiment, the drive level applied to the gate electrode may be controlled using a transistor/resistor combination. Where the Q2 source electrode needs to be biased negative with respect to ground, the transistor Q6 and the resistor R3 pro-

vide level shifting in the negative direction.

The high-side driver/level shifter 110 includes a transistor Q7 (e.g., a P-FET) coupled between an operational voltage V_{SS} ($V_{SS} > V_{DD}$) and the gate of the transistor Q5. During the ON portion of the duty cycle, the transistor Q7 is turned on, raising the gate of the transistor Q5 and causing it to turn on. A remaining portion of the high-side driver/level shifter performs a level-shifting function, allowing the transistor Q7 to be controlled using a logic-level signal. In particular, a resistive voltage divider network (series-connected resistors R1 and R2) is coupled from the voltage V_{SS} through a transistor Q1 to ground. An intermediate node between the resistors R1 and R2 is coupled to a gate electrode of the transistor Q7. When the transistor Q1 is turned on, current flows through the voltage divider, causing a voltage to be applied to the gate of the transistor Q7 sufficient to turn it on.

One of the challenges presented in designing the level-shifting circuit is to maintain efficiency. A capacitor C1 coupled in parallel with the resistor R1 improves efficiency.

More particularly, the driving impedance for the gate of transistor Q7 must be minimized to rapidly switch on the transistor Q7. The turn-off time, on the other hand, can be as long as the period of the minimum allowed duty cycle for the power supply.

Without the capacitor C1, the driving impedance in the ON direction for the gate of the transistor Q7 is the ON resistance, Rds, of the transistor Q1 plus the resistance R1. It would be easy to minimize this impedance by making the resistor R1 equal to zero. However, the DC current through R1 and R2 would then be very high for as long as the transistor Q1 is ON. The value of the resistor R2 is chosen such that its combination with the gate-to-source capacitance, Cgs, of the transistor Q7 makes an RC time constant low enough to meet the minimum duty cycle requirement.

Adding the capacitor C1 momentarily lowers the drive impedance for the gate of the transistor Q7 down to the sum of the ON resistance of the transistor Q1 and the effective series resistance (ESR) of the capacitor C1. The capacitance Cgs of the transistor Q7 can then be charged up rapidly. The value of the capacitor C1 may be chosen to be approximately equal to the value of the capacitance Cgs of the transistor Q7. The value of the resis-

tor R1 can then be made as high as that of the resistor R2, which makes the DC current smaller and increases efficiency.

A waveform diagram illustrating operation of the circuit of Figure 1 is shown in Figure 2, showing waveforms applied to the gate electrodes of the transistors Q1 and Q6 in order to produce a waveform of the desired duty cycle on the gate electrode of the transistor Q5. As may be observed, the gate electrode of the transistor Q5 goes high when the gate electrode of the transistor Q1 goes high, and is driven low when the gate electrode of the transistor Q6 is driven low. To ensure non-overlapping operation of the transistors Q7 and Q2, the gate electrode of the transistor Q6 is raised (turning the transistor Q6 off) some small time before the gate electrode of the transistor Q1 is raised (turning the transistor Q1 on). Similarly, the gate electrode of the transistor Q1 is lowered (turning the transistor Q1 off) some small time before the gate electrode of the transistor Q6 is lowered (turning the transistor Q6 on).

The power consumption of the circuit of Figure 1 is greater than desired. In particular, considerable power is dissipated by the resistive voltage divider network during the time that the gate electrode of the transistor Q1 is high.

Furthermore, the upper frequency limit at which the circuit of Figure 1 can be operated is lower than desired. Where the switch mode power supply is used in next-generation wireless telecommunications applications, for example, it is desirable for the switch mode power supply to be able to track envelope variations of the telecommunications signal, requiring in some instances switching speeds upward of 2MHz.

French Patent 2,768,574 also describes a switched-mode power amplifier arrangement. Referring to Figure 9, in this arrangement, the power amplifier circuit comprises a DC-to-DC converter 20 and a power amplifier 30. The DC-to-DC converter 20 includes a pulse-width modulator 22, a commutator/rectifier 24 and a filter 26.

The pulse-width modulator 22 is coupled to receive a DC-to-DC command input signal from a signal input terminal 21, and is arranged to apply a pulse-width-modulated signal to the commutator/rectifier 24. The commutator/rectifier 24 is coupled to receive a

DC-to-DC power supply input signal from a signal input terminal 25, and is also coupled to apply a switched signal to filter 26. The filter 26 in turn applies a filtered switched signal 28 in common to multiple stages of the power amplifier 30.

A circuit of the foregoing type is substantially limited by the frequency of the pulse-width modulator. In addition, common control of multiple power amplifier stages in the manner described may prove disadvantageous as described more fully hereinafter.

SUMMARY OF THE INVENTION

The present invention, generally speaking, provides a power-efficient method of driving a switch mode power supply at higher frequencies than those typically attainable in the prior art. In an exemplary embodiment, driver transistors exhibit gate capacitance, which is exploited by charging the gate capacitance using a pulse signal and thereafter allowing the gate capacitance to discharge. With the gate capacitance charged, the driver transistor remains on for the desired period of time even without a drive signal being continuously applied, thus conserving power. In essence, the gate capacitance is exploited in the manner of a memory cell. Furthermore, at higher-frequency operation, instead of the gate capacitance being fully charged, leading to increased turn-off time, the gate capacitance is only partially charged, allowing for quicker turn around. The envelope-following capability of the switch mode power supply, in telecommunications applications, is therefore increased. In accordance with another aspect of the invention, in RF amplification circuit having a phase path and a magnitude path, an amplifier is provided having at least a final stage, the amplifier having an RF input coupled to the phase path; and a switch mode power supply is coupled to an operational voltage and to a power supply input terminal of the amplifier. The switch mode power supply includes a transistor switch, a driver circuit for driving the transistor switch, and a controller, the controller causing the driver circuit to operate in charge transfer mode in which a pulse of short duration relative to a duty cycle of the switch mode power supply is used to turn on the transistor switch.

BRIEF DESCRIPTION OF THE DRAWING

The present invention may be further understood from the following description in conjunction with the appended drawing. In the drawing:

Figure 1 is a diagram of a known switch mode power supply and driver circuit;

Figure 2 is a waveform diagram illustrating conventional operation of the circuit of Figure 1;

Figure 3 is a diagram of a switch mode power supply in which a parasitic gate capacitance is used to advantage;

Figure 4 is a waveform diagram illustrating the method of the invention in an exemplary embodiment thereof;

Figure 5 is a diagram of an alternative embodiment of a switch mode power supply and driver circuit with which the present invention may be used;

Figure 6 is a waveform diagram illustrating operation of the circuit of Figure 5;

Figure 7 is a graph comparing power dissipation of a prior art driving circuit and method with the driving circuit and method of the present invention in one embodiment thereof;

Figure 8 is a diagram of an RF power amplifier in accordance with another aspect of the present invention; and

Figure 9 is a diagram of a known RF power amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Figure 3 and Figure 4, a diagram is shown of a switch mode power supply in which a parasitic gate capacitance $C_{gs,5}$ is used to advantage (Figure 3), together with a waveform diagram (Figure 4) illustrating the method of the invention in an exemplary embodiment thereof. To reduce power consumption in the resistive divider network of the circuit of Figure 1, the time for which the gate electrode of the transistor Q1 is held high is minimized. In particular, the gate electrode of the transistor Q1 is pulsed high for a length of time calculated to charge the parasitic gate capacitance of the transistor Q5 and maintain the transistor in the ON state for up to the maximum expected positive portion of duty cycle.

At the point in time when the transistor Q5 is to be turned off, the gate electrode of the transistor Q6 is pulsed low, discharging the parasitic gate capacitance of the transistor Q5 and causing it to turn off.

Referring still to Figure 4, the driver circuit alternates between three states, a charge transfer state (A), a charge removal state (B), and a high-impedance state (Z). The driver occupies states A and B only briefly; otherwise, the driver occupies state Z, the high-impedance state. Significant power dissipation occurs only in state A, and the time spent in state A is minimized.

In the foregoing arrangement, the capacitance of the main switch is used, in effect, as a one-bit memory element. That is, the circuit is operated in charge transfer mode, where the objective is to transfer a finite amount of charge from one place (the driver) to another (the switch) or back again. This manner of operation is entirely different from providing a voltage, or a current, on a circuit node.

Note that the parasitic capacitance need not be fully charged, as typically occurs in the prior art. Therefore, higher frequency operation may be obtained.

To avoid losses occurring in the Schottky diode D1 and achieve still greater efficiency, the Schottky diode D1 may be replaced by the circuit of Figure 5 to achieve synchronous rectification. In this arrangement, a clamping transistor (switch) Q8 is substituted for the Schottky diode D1, being coupled from a source electrode of the transistor Q5 (Figure 1) to ground and controlled by the combination of a charge source transistor Q9 and a charge removal transistor Q10. A fast-junction clamp diode D1' is still coupled to the circuit node N, but its forward voltage is not critical.

Referring to Figure 6, in operation, the transistor Q8 is turned on (making a connection to ground) when the transistor Q5 is turned OFF.

More particularly, when the transistor Q5 is turned OFF, the magnetic field in the inductor L1 collapses, inducing a reverse voltage across it. In the case of the circuit of Figure 3, this reverse voltage forward biases the Schottky diode, and current flow is maintained through the output and the load. Losses in the Schottky diode are significant (P = Vf * I).

The forward voltage drop is typically in the 0.5 to 1.0V range, and the current I may be in the 5A range. This loss is minimized in the circuit of Figure 5 by turning ON the transistor Q8 which, in the ON condition, has a small voltage drop; e.g., Vf approaches 0.01V, while the current remains as before. Clamp power losses therefore drop by up to 1 - 0.01/1 = 99%, easily justifying the additional parts and slightly more complicated circuitry of Figure 5.

The transistors Q9 and Q10 may be driven using the same method as with transistors Q1 and Q6. That is, when the transistor Q8 is to be turned on, the gate electrode of the transistor Q9 is pulsed; when the transistor Q8 is to be turned off, the gate electrode of the transistor Q10 is pulsed.

Figure 7 is a graph comparing power dissipation of a prior art driving circuit and method (e.g., Figure 1 and Figure 2) with the driving circuit and method of the present invention (e.g., Figure 3 and Figure 4) in one embodiment thereof. Here, F = 2.4MHz and V_{DD} = 30.5V. At very low duty cycles, power dissipation of the two circuits is roughly equal. Thereafter, whereas power dissipation of the prior art circuit increases roughly linearly with increasing duty cycle, power dissipation in accordance with the teachings of the present invention remains constant with increasing duty cycle.

By operating the driver circuit for a switch mode power supply in charge-transfer mode, and placing the driver circuit in a high-output-impedance state at all other times, driver power consumption is dramatically decreased. Charge-transfer mode allows the driver duty cycle to become very low. High speed operation (2MHz and above) is therefore made possible, at high voltage (e.g., 30V) and high current (e.g., 5A). The principles of the present invention apply not only to buck converters but to a wide variety of implementations and modes including buck, boost, synchronous rectification, etc., both alone and in combination.

Referring now to Figure 8, a diagram of an RF power amplifier in accordance with another aspect of the present invention. As compared to the known power amplifier of Figure 9, the power amplifier of Figure 8 uses a switch mode power supply in accordance with the previous teaching of the present description. Accordingly, the envelope-following capa-

bility of the switch mode power supply is therefore increased. Furthermore, provision is made for independent control of the power supplies of the multiple stages of the power amplifier. Further details of such independent control may be found in U.S. Patent 6,256,482, in U.S. Patent Application 09/684,497, and U.S. Patent Application 09/834,024, all of which are incorporated herein by reference, addressing efficiency of cascaded stages, the reduction of AM/PM distortion, and precise power control over a wide dynamic range.

In particular, the power supply voltages (or currents) for the respective stages of the amplifier in Figure 8 are separately controlled by separate control circuitry. The control circuitry for the final stage includes a switch mode power supply (SMPS) as previously described. The control circuitry for the preceding driver stage is preferably also provided with such a switch mode power supply, and the pre-driver stage may also be so provided.

The same control mechanism may be used to perform modulation, burst control and power level control, as described in further detail in U.S. Patent Application 09/637,269, incorporated herein by reference.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range of equivalents thereof are intended to be embraced therein.